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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/728,570	12/05/2003	Marcus D. Riedel	18021-6226	8898

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EXAMINER	
LIN, SUN J	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 03/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/728,570	RIEDEL ET AL.	
	Examiner	Art Unit	
	Sun J. Lin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/05/2003 and 07/16/2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-71* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17,19,20,47-66,68 and 69* is/are rejected.

7)☒ Claim(s) *18,21-46,67,70 and 71* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 December 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/2/04,8/30/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/728,570 filed on 12/05/2003.

Claims 1 – 71 remain pending in the application.

Specification Objections

2. The specification is objected to because of following informalities:

Page 6, verification of cyclic functions below line 13 is required, specifically expression for cyclic parameter b, based on data in truth table in Fig. 1.
Page 7, verification of cyclic functions below line 5 is required, specifically expression for cyclic parameter b, based on data in truth table in Fig. 1.

Appropriate corrections are required.

Drawing Objections

3. Drawings are objected to because of following informalities:

Figure 1 should be labeled as a —(PRIOR ART)—.
Figure 2, correct expression for b, based on data in truth table in Figure 1.
Figure 25, based on equation shown, direction of a arrow line between f2 and f3 should be reversed.

Appropriate correction is required.

Claim Objections

4. Claims listed below are objected to because of the following informalities:

Claim 1, line 2, change "parameter" to —**parameters**—.
Claim 1, line 3, change "a combinational circuit" to —**the combinational circuit**—.
Claim 2, line 1, change A method" to —**The method**—.
Claim 2, line 1, before "determining" insert —**the**—.
Claim 2, line 5, before "at least one output" insert —**the**—.
Claim 3, line 1, change A method" to —**The method**—.
Claim 4, line 1, change A method" to —**The method**—.
Claim 4, line 2, after "input" insert —**variable**—.

Claim 4, line 2, before "output" insert —**an**—.
Claim 5, line 1, change A method" to —**The method**—.
Claim 5, line 1, before "determining" insert —**the**—.
Claim 5, line 5 – 6, before "at least one internal variable" insert —**the**—.
Claim 6, line 1, change A method" to —**The method**—.
Claim 6, line 1, before "at least one internal variable" insert —**the**—.
Claim 7, line 1, change A method" to —**The method**—.
Claim 7, line 2, after "input" insert —**variable**—.
Claim 7, line 2, before "internal" insert —**an**—.
Claim 8, line 1, change A method" to —**The method**—.
Claim 8, line 1, before "cyclic parameter" insert —**determined**—.
Claim 9, line 1, change A method" to —**The method**—.
Claim 9, line 1, before "cyclic parameter" insert —**determined**—.
Claim 10, line 1, change A method" to —**The method**—.
Claim 11, line 1, change A method" to —**The method**—.
Claim 12, line 1, change A method" to —**The method**—.
Claim 13, line 1, change A method" to —**The method**—.
Claim 14, line 1, change A method" to —**The method**—.
Claim 15, line 1, change A method" to —**The method**—.
Claim 16, line 1, change A method" to —**The method**—.
Claim 17, line 1, change A method" to —**The method**—.
Claim 18, line 1, change A method" to —**The method**—.
Claim 19, line 1, change A method" to —**The method**—.
Claim 20, line 1, change A method" to —**The method**—.
Claim 21, line 1, change A method" to —**The method**—.
Claim 21, line 1, before "synthesizing" insert —**the**—.
Claim 22, line 1, change A method" to —**The method**—.
Claim 23, line 1, change A method" to —**The method**—.
Claim 24, line 1, change A method" to —**The method**—.
Claim 25, line 1, change A method" to —**The method**—.
Claim 26, line 1, change A method" to —**The method**—.
Claim 27, line 1, change A method" to —**The method**—.
Claim 28, line 1, change A method" to —**The method**—.
Claim 29, line 1, change A method" to —**The method**—.

Claim 30, line 1, change A method" to —**The method**—.
Claim 31, line 1, change A method" to —**The method**—.
Claim 32, line 1, before "introducing" insert —**the**—.
Claim 32, line 1, before "determining" insert —**the**—.
Claim 32, line 2, before "repeating" insert —**the**—.
Claim 32, line 2, change "is" to —**are**—.
Claim 33, line 1, change A method" to —**The method**—.
Claim 34, line 1, change A method" to —**The method**—.
Claim 34, line 1, before "synthesizing" insert —**the**—.
Claim 34, line 3, before "network" insert —**densely interconnected**—.
Claim 34, line 4, before "network" insert —**densely interconnected**—.
Claim 34, line 5, before "excluding" insert —**the**—.
Claim 34, line 5, change "the network" to —**from the densely interconnected**—
Claim 35, line 1, change A method" to —**The method**—.
Claim 35, line 1, before "combinational circuit" insert —**desired**—.
Claim 36, line 1, change A method" to —**The method**—.
Claim 36, line 1, before "combinational circuit" insert —**desired**—.
Claim 37, line 1, change A method" to —**The method**—.
Claim 38, line 1, change A method" to —**The method**—.
Claim 39, line 1, change A method" to —**The method**—.
Claim 40, line 1, change A method" to —**The method**—.
Claim 40, line 1, before "combinational circuit" insert —**desired**—.
Claim 41, line 1, change A method" to —**The method**—.
Claim 42, line 1, change A method" to —**The method**—.
Claim 42, line 1, before "combinational circuit" insert —**desired**—.
Claim 43, line 1, change A method" to —**The method**—.
Claim 43, line 1, before "combinational circuit" insert —**desired**—.
Claim 44, line 1, change A method" to —**The method**—.
Claim 44, line 1, before "combinational circuit" insert —**desired**—.
Claim 45, line 1, before "introducing" insert —**the**—.
Claim 45, line 1, before "determining" insert —**the**—.
Claim 45, line 2, before "repeating" insert —**the**—.
Claim 48, line 1, change A method" to —**The method**—.
Claim 48, line 1, before "cyclic parameter" insert —**determined**—.

Claim 49, line 1, change A method" to —**The method**—.
Claim 50, line 2, before "a set of" insert —**a logic for determining**—.
Claim 50, line 4, after "determined" insert —**set of**—.
Claim 51, line 1, change "A synthesizer" to —**The logic synthesizer**—.
Claim 51, line 1, before "cyclic parameters" insert —**determined set of**—.
Claim 51, line 5, after "input" insert —**variable**—.
Claim 51, line 5, before "at least one output variable" insert —**the**—.
Claim 52, line 1, change "A synthesizer" to —**The logic synthesizer**—.
Claim 53, line 1, change "A synthesizer" to —**The logic synthesizer**—.
Claim 53, line 2, after "input" insert —**variable**—.
Claim 53, line 2, before "output variable" insert —**an**—.
Claim 54, line 1, change "A synthesizer" to —**The logic synthesizer**—.
Claim 54, line 1, before "cyclic parameter" insert —**determined set of**—.
Claim 54, line 5, after "input" insert —**variable**—.
Claim 54, line 5, before "at least one internal" insert —**the**—.
Claim 55, line 1, change "A synthesizer" to —**The logic synthesizer**—.
Claim 55, line 1, before "at least one" insert —**the**—.
Claim 56, line 1, change "A synthesizer" to —**The logic synthesizer**—.
Claim 56, line 2, after "input" insert —**variable**—.
Claim 56, line 2, before "internal variable" insert —**an**—.
Claim 57, line 1, change "A synthesizer" to —**The logic synthesizer**—.
Claim 57, line 1, before "cyclic parameter" insert —**determined set of**—.
Claim 58, line 1, change "A synthesizer" to —**The logic synthesizer**—.
Claim 58, line 1, before "cyclic parameter" insert —**determined set of**—.
Claim 59, line 1, change "A synthesizer" to —**The logic synthesizer**—.
Claim 60, line 1, change "A synthesizer" to —**The logic synthesizer**—.
Claim 61, line 1, change "A synthesizer" to —**The logic synthesizer**—.
Claim 62, line 1, change "A synthesizer" to —**The logic synthesizer**—.
Claim 63, line 1, change "A synthesizer" to —**The logic synthesizer**—.
Claim 64, line 1, change "A synthesizer" to —**The logic synthesizer**—.
Claim 65, line 1, change "A synthesizer" to —**The logic synthesizer**—.
Claim 66, line 1, change "A synthesizer" to —**The logic synthesizer**—.
Claim 67, line 1, change "A synthesizer" to —**The logic synthesizer**—.
Claim 68, line 1, change "A synthesizer" to —**The logic synthesizer**—.

Claim 69, line 1, change "A synthesizer" to —**The logic synthesizer**—.
Claim 70, line 1, change "A synthesizer" to —**The logic synthesizer**—.
Claim 70, line 4, change "circuit," to —**circuit**—.
Claim 71, line 1, change "A synthesizer" to —**The logic synthesizer**—.
Claim 71, line 2, change "the network" to —**the densely interconnected**—.
Claim 71, line 3, change "the network" to —**the densely interconnected**—.
Claim 71, line 3 – 4, change "the network" to —**the densely interconnected**—.

Appropriate corrections are required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1 – 13, 19, 20, 47 – 62, 64 – 66, 68 and 69 are rejected under 35 U.S.C. 102(b) as being unpatentable over applicants' submitted IDS, paper entitled "*Constructive Analysis of Cyclic Circuits*" authored by *Shiple et al.*

7. As to Claim 1, *Shiple et al.* show and teach the following subject matter:

- A combination circuit whose inputs and outputs are defined by a set of equations containing parameters x and y – [Fig. 1; Section 1.1 Well-behaved cyclic circuits]; Notice that (1) x and y are a set of cyclic parameters (2) output of each logic gate (e.g., x for upper gate, y for lower gate) can be defined as a cyclic parameter;
- Building (i.e., synthesizing) combinational circuit...cyclic combinational circuits – [Section 1: Introduction]; Hardware and software synthesis (i.e., logic synthesis process) of cyclic combinational circuits – [title; abstract]; Notice that a combinational circuit is synthesized in accordance with the cyclic parameters x and y.

For reference purposes, the explanations given above in response to Claim 1 are called **[Response A]** hereinafter.

8. As to Claims 47 and 50, reasons are included in **[Response A]** given above.

9. As to Claims 2 – 4 and 51 – 53, in addition to reasons included in **[Response A]** given above, *Shiple et al.* show the following subject matter in equations in Section 1.1 Well-behaved Cyclic Circuits:

- Cyclic parameter y is an input variable to a upper logic gate in Fig. 1(a);
- Cyclic parameter x is an output variable to a upper logic gate in Fig. 1(a);
- Cyclic parameter x is an input variable to a lower logic gate in Fig. 1(a);
- Cyclic parameter y is an output variable to a lower logic gate in Fig. 1(a);
- Two equations, which define a relationship between x and y whereby the relationship includes a cycle;
- Due to the fact that output of each logic gate can be defined as a cyclic parameter, the cyclic parameter can be an internal variable – [Fig. 3];
- There is a structured dependency between an input variable and an output variable – [Fig. 1; Fig. 3].

For reference purposes, the explanations given above in response to Claim 2 – 4 and 51 – 53 are called **[Response B]** hereinafter.

10. As to Claims 5 – 7 and 54 – 56, in addition to reasons **[Response B]** included in given above, *Shiple et al.* show and disclose the subject matter in – [Fig. 1; Fig. 3; Section 1.1]

11. As to Claims 8 – 10, 48, 49 and 57 – 59, in addition to reasons included in **[Response A]** given above, *Shiple et al.* teach the following subject matter:

- Combinational loops (i.e., cyclic loops in cyclic combinational circuits) can be useful...cyclic circuits can be used to *reduce circuit size* – [abstract]. Notice that the cyclic parameters can be applied in building a *cyclic combinational circuit (building block)* for use in substitution phase of structuring operation of a logic synthesis process in order to *minimize (i.e., optimize) overall size* of a logic circuit under study.

For reference purposes, the explanations given above in response to Claims 8 – 10, 48, 49 and 57 – 59 are called **[Response C]** hereinafter.

12. As to Claims 11, 16, 17, 20, 60, 65, 66 and 69, *Shiple et al.* teach the following subject matter:

- Referring to Fig. 1(a), the cyclic (combinational) circuit is stabilized (i.e., optimized) if both inputs a, b are not 1 – [Section 1.1]; Notice that the cyclic (combinational) circuit is stabilized (optimized) with regard to electrical behavior (i.e., performance);
- Output of the cyclic (combinational) circuit is stabilized for all *wire delay* – [Section 1.1].
- Stabilization of electrical behavior with regard to testability.

13. As to Claims 12, 13, 15, 19, 61, 62, 64 and 68 in addition to stabilize electrical behavior, *Shiple et al.* teach subject matter in **[Response C]** given above regarding reducing (optimizing) circuit size (i.e., area) by using cyclic circuits. Notice that (1) reducing the size is reducing cost of a logic circuit (2) the size of a logic circuit is reduced by reducing a gate count (3) reducing a gate count will minimize power consumption of the logic circuit.

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

(1). Determining the scope and contents of the prior art.
(2). Ascertaining the differences between the prior art and the claims at issue.
(3). Resolving the level of ordinary skill in the pertinent art.
(4). Considering objective evidence present in the application indicating obviousness or nonobviousness.

15. Claims 14 and 63 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicants' submitted IDS, paper entitled "*Constructive Analysis of Cyclic Circuits*" authored by *Shiple et al.* in view of U.S. Patent No. 5,515,292 to *Roy et al.*

16. As to Claim 14, *Shiple et al.* disclose a combinational circuit is optimized with regard to cost, which is measured as an area (size), they do not teach that the area is determined by literal count. But *Roy et al.* disclose that, in combinational logic (circuit) synthesis, literal count is reduced in order to achieve area saving, which is very important in minimizing the cost of manufacturing a combinational logic circuit – [col. 6, line 53 – col. 7, line 32].

Therefore it would have been obvious at the time the invention was made to a person having ordinary skill to have applied the teachings of *Roy et al.* in reducing literal count of a combinational logic circuit in order to achieve area saving thereby minimizing the cost of manufacturing the combinational logic circuit.

For reference purposes, the explanations given above in response to Claim 14 are called **[Response D]** hereinafter.

17. As to Claim 63, reasons are included in **[Response D]** given above.

Allowable Subject Matter

18. Claims 18, 21 – 46, 67, 70 and 71 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Those claims are allowed because that the prior art does not teach or fairly suggest the following subject matter:

- A method of producing a combinational circuit, the method comprising *producing a combinational circuit that is optimized with regard to fault tolerance* in combination with other limitations as recited in **Claim 18**;
- A logic synthesizer comprising a processor configured to *synthesize a combinational circuit that is optimized with regard to fault tolerance* in combination with other limitations as recited in **Claim 67**;

- A method of producing a combinational circuit, the method comprising *synthesizing a combinational circuit by creating a network with no cycle, introducing a cycle into the network, determining if the network is combinational and repeating introduction of cycles into the network until a desired combination circuit is implemented* in combination with other limitations as recited in **Claim 21**;
- A method of producing a combinational circuit, the method comprising *synthesizing a combinational circuit by creating a densely interconnected network, excluding edges from the densely interconnected network, determining if the densely interconnected network is combinational and repeating excluding edges from the densely interconnected network until a desired combination circuit is implemented* in combination with other limitations as recited in **Claim 34**;
- A logic synthesizer comprising *a processor that creates a network with no cycle, and then introduces a cycle into the network and determines if the network is combinational and then repeats introducing of cycles into the network until a desired combination circuit is implemented* in combination with other limitations as recited in **Claim 70**;
- A logic synthesizer comprising *a processor that creates a densely interconnected network, and then excludes edges from the densely interconnected network and determines if the densely interconnected network is combinational and the repeats excluding edges from the densely interconnected network until a desired combination circuit is implemented* in combination with other limitations as recited in **Claim 71**.

Conclusion

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to *Sun James Lin* whose telephone number is (571) 272 - 1899. The examiner can normally be reached on Monday-Friday 9:30AM - 6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, *Jack Chiang* can be reached on (571) 272 - 7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sun James Lin
Patent Examiner
Art Unit 2825
March 9, 2006